Other embodiments include using both UV and electron beam cures.

Still other embodiments are in the following claims.

WHAT IS CLAIMED IS:

5

1. A method of forming an integrated circuit, including forming a dielectric film comprising,

providing a substrate,

providing a CDO film on the substrate, and

treating the CDO film with an electron beam.

2. The method of claim 1 wherein the energy of the electrons in the electron beam is about 3 keV or greater.

3. The method of claim 1 wherein the energy of the electrons in the electron beam is about 8 keV or greater.

4. The method of claim 1 wherein the energy of the electrons in the electron beam is determined such that the predicted Kanaya-Okayama range of the electrons exceeds the thickness of the CDO film.

5. The method of claim 1 comprising,

preparing the CDO film on the substrate by using chemical vapor deposition.

6. The method of claim 1 wherein the dielectric film is an interlevel dielectric film comprising,

preparing a damascene structure in the CDO film.

7. The method of claim 6 comprising,

filling the damascene structure with a metal.

8. The method claim 7 comprising,

removing excess metal by using chemical, mechanical polishing (CMP).

9. The method of claim 8 wherein the metal is copper.

10. An integrated circuit, including a dielectric film comprising a CDO film having a modulus of about 20 GPa or greater.

11. The integrated circuit of claim 10 wherein the CDO film has a dielectric constant of about 2 to about 4.

12. The integrated circuit of claim 10 wherein the CDO film has a dielectric constant less than about 3.

13. The integrated circuit of claim 10 wherein the CDO film has a density less than about 2 g/cm^3.

14. The integrated circuit of claim 10 wherein the CDO film has a density of about 1.3 g/cm^3 to about 1.4 g/cm^3.

15. The integrated circuit of claim 11 wherein the dielectric film is an interlevel dielectric film.

16. The integrated circuit of claim 10 wherein the film has a modulus of about 20 GPa to about 25 GPa.

17. The integrated circuit of claim 16 wherein the dielectric constant is about 2 to about 4.

18. The integrated circuit of claim 17 wherein the dielectric film is an interlevel dielectric film.

19. An integrated circuit, including a dielectric film comprising a CDO film having a hardness of about 2.8 GPa or greater.

20. The integrated circuit of claim 19 wherein the CDO film has a dielectric constant of about 2 to about 4.

21. The integrated circuit of claim 20 wherein the dielectric film is an interlevel dielectric film.

22. The integrated circuit of claim 19 wherein the film has a hardness of about 2.8 GPa to about 3.5 GPa.

23. The integrated circuit of claim 22 wherein the CDO film has a dielectric constant of about 2 to about 4.

24. The integrated circuit of claim 23 wherein the dielectric film is an interlevel dielectric film.

25. An integrated circuit, including a dielectric film comprising a CDO film having a hardness of about 2.8 GPa or greater and a modulus of about 20 GPa or greater.

26. The integrated circuit of claim 25 wherein the CDO film has a hardness of about 2.8 GPa to about 3.5 GPa and a modulus of about 20 GPa to about 25 GPa.

27. The integrated circuit of claim 26 wherein the CDO film has a dielectric constant of about 2 to about 4.

28. The integrated circuit of claim 27 wherein the dielectric film is an interlevel dielectric film.